DESIGN SHOWCASE

MOSFET Pass Element Yields 100mV-Dropout Regulator

In terms of low R_{ON}, the best pass transistor for a low-dropout, positive-voltage regulator is an N-channel MOSFET. All such commercially available regulators, however, use bipolar PNP pass transistors. The PNP transistor can saturate completely in these applications because the base voltage is lower than the output voltage, producing a collector-emitter voltage of less than 0.4V. For comparison, the corresponding drop across an NPN pass transistor is greater than $V_{BE(SAT)}$ (1.2V minimum) because regulator circuits generally provide no base-drive voltage higher than the input (V_{CC}).

N-channel MOSFETs provide the lowest $V_{DROP} = I_{OUT} \times R_{ON}$, but the required V_{GS} drive varies with output current and ranges 3 to 4 volts above the output voltage. In **Fig 1**, the circuit provides this drive voltage by employing a voltage-converter chip (IC1) that uses charge-pump techniques to boost a 5V input to 10V. The 10V output then drives a positive-voltage requlator (IC2), which in turn drives the N-channel, logic-level MOSFET Q1. The gate drive available to Q1 remains high (10V) because the low supply current into IC2 (10µA) produces a small IR drop through IC1 (approximately 1.5mV), which enables IC1's output to remain nearly twice the value of V_{CC}.

During operation at 500mA, the dropout voltage – the minimum value of V_{CC}-V_{OUT} that sustains regulation – is only 100mV. The quiescent current is only 1mA, thanks to the CMOS technology of IC1 and IC2. Resistor R3 prevents the MOSFET gate from floating when the regulator is OFF, and the feedback resistors R1 and R2 set the regulator's output voltage V_{OUT}:

$$V_{OUT} = 1.3V \frac{(R1+R2)}{R1}$$

IC2 also incorporates a low-battery detector whose output (LBO) goes low when the detector's input voltage (connected to LBI) goes below 1.3V. As shown, the circuit detects V_{CC} overvoltage. LBO remains low for normal-range V_{CC} levels and goes high when V_{CC} exceeds its upper limit (6.3V in this case). IC2 shuts down when LBO pulls the SHDN input high, thereby preventing excessive dissipation in the pass transistor by removing its gate drive. R7 protects IC1 by restricting its current flow.

You can also use the detector to sense complete saturation in Q1 (the condition in which V_{CC} is less than V_{OUT} plus 100mV). Connect SHDN to ground. (Or, you can turn the output off and on by driving SHDN with a CMOS gate.) Set the R5-R6 divider to produce 1.3V when $V_{CC} = V_{OUT}$+100mV, and then monitor LBO for the low (fault) condition.